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Patent

Attorney Docket No.: 2207/618602
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant No.	:	10/659,133 Confirmation No. 4796
Applicants	:	Per HAMMARLUND et al.
Filed	:	September 10, 2003
For	:	ACCESS CONTROL OF A RESOURCE SHARED BETWEEN COMPONENTS
Group Art Unit	:	2161
Examiner	:	Te Y CHEN
Customer No.	:	25693

M/S: APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING

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Dated: November 17, 2006

Blanche Guzman-Salmon

ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on August 17, 2006.

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1. REAL PARTY IN INTEREST

The real party in interest in this matter is Intel Corporation. (Recorded June 7, 1999; Reel/Frame 010050/0320).

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals.

3. STATUS OF THE CLAIMS

Claims 2-11, 13, 18, and 20 are pending in the application. Claims 2-11, 13, 18, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,644,753) in view of Arimilli et al. (U.S. Patent No. 5,867,511).

4. STATUS OF AMENDMENTS

The claims listed on page A-1 of the Appendix attached to this Appeal Brief reflect the present status of the claims.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The embodiment of independent claim 2 generally describes an apparatus, comprising: a resource having a plurality of elements (*see eg.* page 5, lines 2-3; figure 1), wherein the elements of said resource are selectively partitioned (*see eg.* page 8, lines 7-8); and at least first and second components to access the elements of said resource and an access controller coupled to said resource and said at least first and second components to store a first mask value (*see eg.* page 5, line 19 – page 6, line 1; figure 1), wherein access to the partitioned elements by said first

and second components is controlled based on said first mask value (*see eg.* page 6, lines 10-13; figure 1).

The embodiment of independent claim 4 generally describes an apparatus comprising: a memory resource having a plurality of addressable blocks (*see eg.* page 6, line 16 – page 7, line 2; figure 2), wherein the addressable blocks of said resource are selectively partitioned (see eg. page 8 lines 7-8); first and second components adapted to access said memory resource (*see eg.* page 5, line 19 – page 6, line 1; figure 1); and an access controller having a register to store a first mask value, wherein access to addressable blocks of partitions is controlled based on said first mask value (*see eg.* page 5, line 19 – page 6, line 1; figure 1).

The embodiment of independent claim 11 generally describes a method comprising: controlling, with an access controller coupled to at least first and second components, which of said at least first and second components are able to access which elements of a selectively partitioned resource (*see eg.* page 18, lines 8-17; figure 4a); and storing in a register of said access controller a first mask value, wherein access to the partitioned elements is controlled based on said first mask value (*see eg.* page 18, lines 8-17; figure 4a).

The embodiment of independent claim 18 generally describes a set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor comprising: controlling, with an access controller coupled to at least first and second components, which of said at least first and second components are able to access which partitions of a selectively partitioned resource (*see eg.* page 5, line 19 – page 6, line 15; figure 1); and storing in a register of said access controller a first mask value, wherein access to the partitioned elements is controlled based on said first mask value (*see eg.* page 5, line 19 – page 6, line 15; figure 1).

Fig. 1 is a block diagram of a resource system constructed according to an embodiment of the present invention.

Fig. 2 is a block diagram of a memory system incorporating an embodiment of the present invention.

Fig. 3 is a more detailed block diagram of the cache memory of Fig. 1.

Figs. 4a and b are flow diagrams of methods according to embodiments of the present invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 2-11, 13, 18, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,644,753) in view of Arimilli et al. (U.S. Patent No. 5,867,511).

7. ARGUMENT

A. Legal Background

Absent anticipation it may be possible to combine two or more patents together to render a claimed invention obvious, and unpatentable, under 35 U.S.C. § 103(a). In determining whether the claims are unpatentable it is necessary to look at what the references actually teach. "It is impermissible within the framework of § 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." In Re Wesslau, 147 U.S.P.Q. (BNA) 391, 393 (C.C.P.A. 1965). Accordingly, a prior art reference must be considered in its entirety, and portions thereof must be taken in proper context. MPEP §

2141.02; Bausch & Lomb, Inc. v. Barnes-Hind, Inc., 230 U.S.P.Q. (BNA) 416, 419 (Fed. Cir. 1986).

B. Claims 2-11, 13, 18, and 20 are not rendered obvious under 35 U.S.C. § 103(a) by Ebrahim et al. (U.S. Patent No. 5,644,753) in view of Arimilli et al. (U.S. Patent No. 5,867,511).

Claims 2-11, 13, 18, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ebrahim in view of Arimilli. Independent claim 2 of the present application includes the following limitation:

> an access controller coupled to said resource and said at least first and second components to store a first mask value, wherein access to the partitioned elements by said first and second components is controlled based on said first mask value.

Examiner asserts that the mask value in Appellants' claim is taught by the UPANUM field (182) in Ebrahim, which is described as "a 5-bit mask field that specifies the maximum number of UPA ports the System Controller can support." *See* Ebrahim, column 22, lines 8-10. These two and a half lines of description constitute the only description of the UPANUM field. It is not clear where the 5-bit value stored in the UPANUM field comes from, or what exactly it does. Earlier in the detailed description, Ebrahim states that "[each] UPA port 104 is identified by a unique 5-bit value, called the Port ID or UPA_Port_ID (se FIG. 3). This allows a maximum of 32 UPA ports in a system." The fact that the reference states that the system can only handle a maximum of 32 UPA ports makes the function of the UPANUM field all the more unclear.

Nothing cited by Examiner supports his assertion that the UPANUM field teaches the first mask value in Appellants' claim. Appellants' claim clearly states that "access . . . is controlled based on said first mask value." The UPANUM field, as best can be determined from the mere two and a half lines spent describing it, represents nothing more than a system

parameter. The UPANUM field in Ebrahim does not affect a component's access to an element, and therefore it cannot teach the first mask value in Appellants' claim.

The fact that the UPANUM field does not affect a component's access to an element is more clearly illustrated by looking at the principle objective of Ebrahim. Ebrahim teaches a system controller for maintaining cache coherence. *See* abstract. As is typical in the art, Ebrahim discloses logic for detecting a cache hit or a cache miss. Column 2, lines 15-26. The novel part of Ebrahim is that it uses a set of duplicate cache tags to, in certain circumstances, speed up retrieving a cache hit by eliminating cache tag compare steps. Column 3, lines 50-53. As is standard in the art, access to the cache in Ebrahim is determined by whether the system detects a cache hit or a cache miss, not the UPANUM field or anything else that could reasonably be interpreted as teaching the first mask value of Appellants' claim.

The Ebrahim reference, therefore, does not teach "access to the partitioned elements by said first and second components is controlled based on said first mask value," a feature found in each of the pending independent claims. Accordingly, Appellants assert that Ebrahim, either by itself or in combination with Arimilli, does not render Appellants' claimed invention obvious, and Appellants, therefore, respectfully request reversal of the rejection of claims 1-25 under 35 U.S.C. § 103(a).

CONCLUSION

Appellants therefore respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 2-11, 13, 18, and 20, and direct the Examiner to pass the case to issue.

The Examiner is hereby authorized to charge any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon LLP Deposit Account No. 11-0600.

Respectfully submitted,

KENYON & KENYON LLP

Date: November 17, 2006

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APPENDIX

(Brief of Appellants Per Hammarlund et al.
U.S. Patent Application Serial No. 10/659,133)

8. CLAIMS ON APPEAL

1. (Cancelled)

2. An apparatus, comprising:

a resource having a plurality of elements, wherein the elements of said resource are selectively partitioned and;

at least first and second components to access the elements of said resource; and

an access controller coupled to said resource and said at least first and second components to store a first mask value, wherein access to the partitioned elements by said first and second components is controlled based on said first mask value.

3. The apparatus of claim 2 wherein said first mask value represents which of the elements of said resource are available for access for a selected component.

4. An apparatus comprising:

a memory resource having a plurality of addressable blocks, wherein the addressable blocks of said resource are selectively partitioned;

first and second components adapted to access said memory resource; and

an access controller having a register to store a first mask value, wherein access to addressable blocks of partitions is controlled based on said first mask value.

5. The apparatus of claim 4 wherein said memory resource is a cache memory.

6. The apparatus of claim 5 further comprising:

a processor coupled to said cache memory, wherein said first component includes execution of instructions by said processor from a first thread and said second component includes execution of instructions by said processor from a second thread.

7. The apparatus of claim 6 wherein said first mask value represents which of the addressable blocks of said cache memory are available for eviction.

8. The apparatus of claim 7 wherein a first mask value is provided for each of said components, said first mask values indicate which of the addressable blocks of said cache memory are available for eviction for one of said components and which of the addressable blocks of said cache memory are available for eviction for at least two of said components.

9. The apparatus of claim 8 wherein an eviction array is provided indicating the least recently used addressable block of said cache memory and a second mask is provided, said second mask value selecting which bits of said eviction array are used in controlling which of the addressable blocks of said cache memory are available for eviction.

10. The apparatus of claim 6, wherein an eviction array is provided indicating a least recently used addressable block of said cache memory and wherein said first mask value is an auxiliary mask value and said auxiliary mask value represents which of the addressable blocks of said cache memory are available for eviction and selects which bits of said eviction array are used in controlling which of the addressable blocks of said cache memory are available for eviction.

11. A method comprising:

controlling, with an access controller coupled to at least first and second components, which of said at least first and second components are able to access which elements of a selectively partitioned resource; and

storing in a register of said access controller a first mask value, wherein access to the partitioned elements is controlled based on said first mask value.

12. (Cancelled)

13. The method of claim 11 further comprising:

determining which of said first and second components is accessing said resource; and

determining which of the elements of the resource are available for access by the component accessing said resource based on said first mask value.

14-17 (Cancelled)

18. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor comprising:

controlling, with an access controller coupled to at least first and second components, which of said at least first and second components are able to access which partitions of a selectively partitioned resource; and

storing in a register of said access controller a first mask value, wherein access to the partitioned elements is controlled based on said first mask value.

19. (Cancelled)

20. The set of instructions of claim 18, wherein the execution of said set of instructions further comprises:

determining which of said first and second components is accessing said resource; and

determining which of the elements of the resource are available for access by the component accessing said resource based on said first mask value.

21-24 (Cancelled)

9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.